Journal of Power Sources 186 (2009) 252–260

Contents lists available at ScienceDirect

Journal of Power Sources

journal homepage: www.elsevier.com/locate/jpowsour

An experimental investigation into micro-fabricated solid oxide fuel cells with ultra-thin $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_3$ cathodes and yttria-doped zirconia electrolyte films

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ARTICLE INFO

Article history:
Received 29 August 2008
Received in revised form 8 October 2008
Accepted 8 October 2008
Available online 17 October 2008

Keywords:
Solid oxide fuel cell (SOFC)
Lanthanum strontium cobalt iron oxide (LSCF)
Cathode
Thin film
Impedance spectroscopy

ABSTRACT

Thin-film solid oxide fuel cells (SOFCs) were fabricated with both Pt and mixed conducting oxide cathodes using sputtering, lithography, and etching. Each device consists of a 75–150 nm thick yttria-stabilized zirconia (YSZ) electrolyte, a 40–80 nm porous Pt anode, and a cathode of either 15–150 nm dense $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (LSCF) or 130 nm porous Pt. Maximum powers produced by the cells are found to increase with temperature with activation energies of 0.94–1.09 eV. At 500 °C, power densities of 90 and 60 mW cm^{-2} are observed with Pt and LSCF cathodes, respectively, although in some conditions LSCF outperforms Pt. Several device types were fabricated to systematically investigate electrical properties of components of these fuel cells. Micro-fabricated YSZ structures contacted on opposite edges by Pt electrodes were used to study temperature-dependent in-plane conductivity of YSZ as a function of lateral size and top and bottom interfaces. Si/Si_3N_4/Pt and Si/Si_3N_4/Au capacitor structures are fabricated and found to explain certain features observed in impedance spectra of in-plane and fuel cell devices containing silicon nitride layers. The results are of relevance to micro-scale energy conversion devices for portable applications.

1. Introduction

Fuel cells are attractive for their high efficiency, low emissions, and direct production of electricity, however their application has been limited by high cost, system complexity, and limited duty or cycle life [1]. Significant research in polymer electrolyte membrane fuel cells (PEMFCs) and solid oxide fuel cells (SOFCs) is focused on strategies to operate in an intermediate temperature range, roughly 200–600 °C [2]. PEMFCs typically operate below 100 °C, but higher temperature would increase catalytic activity and impurity resistance. SOFCs typically operate above 700 °C, and lower temperature would bring more material flexibility, less corrosive side reactions, quicker thermal cycling, and easier scaling down, and thus may enable SOFCs to power portable electronics or transportation.

Energy conversion in a fuel cell involves a variety of processes in tandem. Some, such as electron transport and gas diffusion, vary little with temperature. Others, such as ion transport and oxidation and reduction reactions, are thermally activated and require significant changes to remain effective as temperature is decreased. Ion transport losses in the electrolyte can be reduced by either increasing conductivity or reducing thickness. Perhaps the most common SOFC electrolyte is yttria-stabilized zirconia (YSZ). While a variety of more conductive electrolyte materials are being investigated [3], the excellent chemical stability of YSZ is prompting efforts to reduce its thickness to the nanoscale [4–6], which may also benefit conductivity [7–12] and surface exchange [5].

In this paper we report on fabrication and measurement of micro-SOFCs with dense thin-film $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (LSCF) cathodes, with performance comparable to their Pt counterparts, as measured from 200 to 600 °C. In addition, we describe various components of these micro-fuel cell chips, in detail that has not been addressed previously. We isolate the variable temperature impedance spectra of the YSZ electrolyte and the silicon nitride insulator, and investigate the structural characteristics of thin-film sputtered LSCF and Pt electrodes. Intermediate temperature YSZ-based SOFCs have previously been made with Pt cathodes [5,13], however Pt degrades quickly at higher temperatures. LSCF and similar materials, such as $Ba_{1-x}Sr_xCo_{1-y}Fe_yO_{3-\delta}$, have garnered substantial attention as intermediate temperature SOFC cathodes [14–16] and LSCF has recently been incorporated into a thin-film fuel cell [6]. These materials are stable at high temperatures, and have the advantage as mixed conductors that the entire surface participates in catalysis, thus a dense film can be used, although nanostructuring can still decrease resistance by increasing surface

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doi:10.1016/j.jpowsour.2008.10.021

area. In addition to being stable at high temperatures, another advantage may be lower cost of ceramic cathode materials compared to precious metals such as Pt.

To the best of our knowledge, this is the first report discussing functional thin-film-based solid oxide fuel cells utilizing RF-sputtered LSCF cathode thin films. Advantages of this approach include thin-film cathode processing approach compatible with photolithography and patterning as well as relative simplicity to synthesize a multi-component, highly dense complex oxide thin film from a single target. Ref. [5] shows that RF sputtered YSZ electrolytes paired with Pt electrodes can make SOFCs with high performance at low temperatures, achieving higher power density than the similar Pt-cathode cells we report here. Ref. [6] describes a similar structure, including both LSCF and Pt as cathode materials, however they deposit the oxide electrolytes and cathodes by pulsed laser deposition (PLD) or spray pyrolysis (SP). Their Pt-cathode cell uses an electrolyte made by one PLD layer and one SP layer to decrease gas leakage and achieve a high open circuit voltage (OCV) and a maximum power nearly identical to that of the Pt-cathode cell we report here. However, the LSCF-cathode cell described in Ref. [6] uses a single PLD layer for the electrolyte. This cell suffers from low OCV and, likely for this reason, lower maximum power than the LSCF-cathode cells we report in this article.

2. Experimental

2.1. Measurement apparatus

At the center of our measurement setup is a hollow stainless steel block, which can be heated to 600 °C. One fuel cell chip, which may contain many individual cells, can be sealed with a gold o-ring over a hole in this block. Through the gold o-ring, the steel block also serves as the common anode connection. Wet forming gas (5% H_2, 3% H_2O, balance Ar) is fed to the anode on the bottom of the chip through a coil of tubing, which thermalizes the gas and equilibrates the $H_2/O_2/H_2O$ system. The top is open to air, and micromanipulator probes with Pt-plated tungsten tips contact the cathodes of individual cells. In-plane conductivity devices can be measured in the same apparatus, by flowing no hydrogen and contacting each electrode with its own micromanipulator probe. Electrical measurements are made either with a Solartron 1260/1287 electrochemical test setup (AC and DC), a Stanford Research 810 lock-in amplifier (AC), or a Keithley 2400 sourcemeter (DC).

2.2. In-plane electrolyte conductivity devices

Fig. 1 shows optical images and schematics of two device geometries used to study the conductivity of thin-film YSZ electrolytes, fabricated similarly to the fuel cell electrolytes and in the presence of the same supporting and insulating materials. Conductivities measured with these devices reflect electrical transport in the plane of the surface, rather than through this plane as in fuel cell devices. The value of these measurements is that it is substantially easier to isolate the electrolyte contribution in an in-plane device than in a through-plane device because the overall resistance of the electrolyte is much greater relative to the electrodes. A reasonable assumption that electrode polarization can be neglected is strongest for the thinnest films with the largest electrode gaps, but was investigated in detail and found to hold for the full range of film thicknesses and temperatures used here by comparing resistances of devices with different electrode gaps.

Both types of device shown in Fig. 1 begin with a 10-mm square silicon chip coated with 1 μm of thermally grown SiO_2. For the devices in Fig. 1(a), rectangles of YSZ are patterned by photolithography, sputtering, and liftoff. For all YSZ and Pt patterning in this article, LOR-3A lift-off resist (Microchem Corp.) and S1813 photoresist (Rohm and Haas Co.) are spun onto the chip and baked (170 and 115 °C, respectively). The pattern is exposed through a photomask, and the S1813 is developed in CD-30 (Rohm and Haas Co.). The chip is baked again at 140 °C, then developed in CD-26 (Rohm and Haas Co.) to etch through and undercut the LOR-3A. After sputtering, the pattern is lifted off in warm (~60 °C) Remover

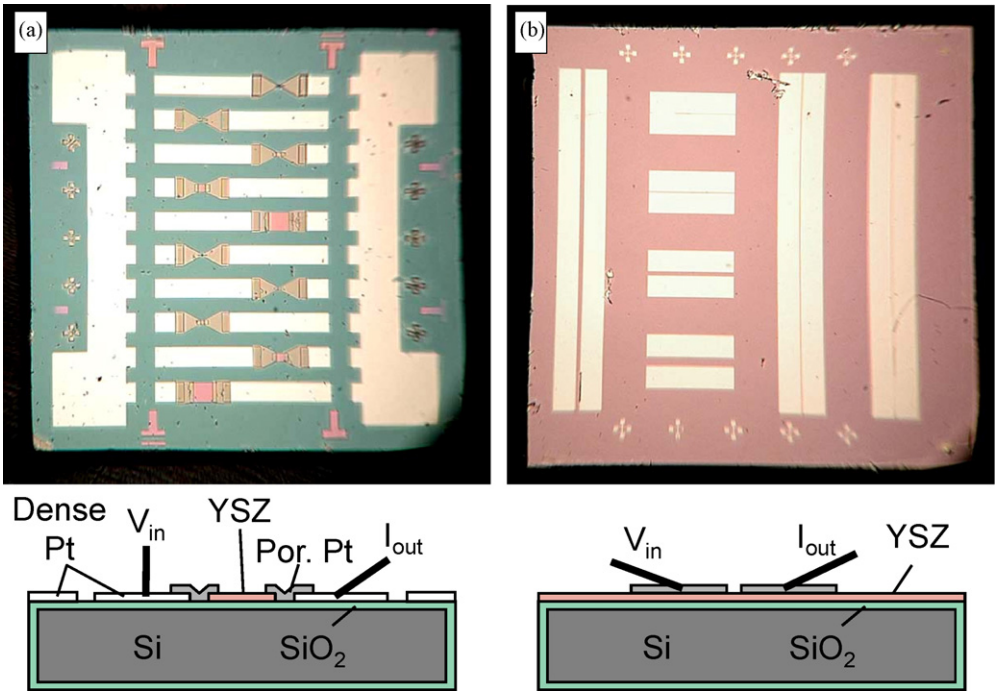

Fig. 1. Optical images and schematics of in-plane conductivity chips. All are Si chips, 10 mm across, coated with approximately 1 μm SiO_2. (a) Square YSZ membranes ranging from 20 to 500 μm contacted by porous Pt, may have Si_3N_4 above or below the YSZ. (b) Strips of porous Pt on a blanket YSZ film.

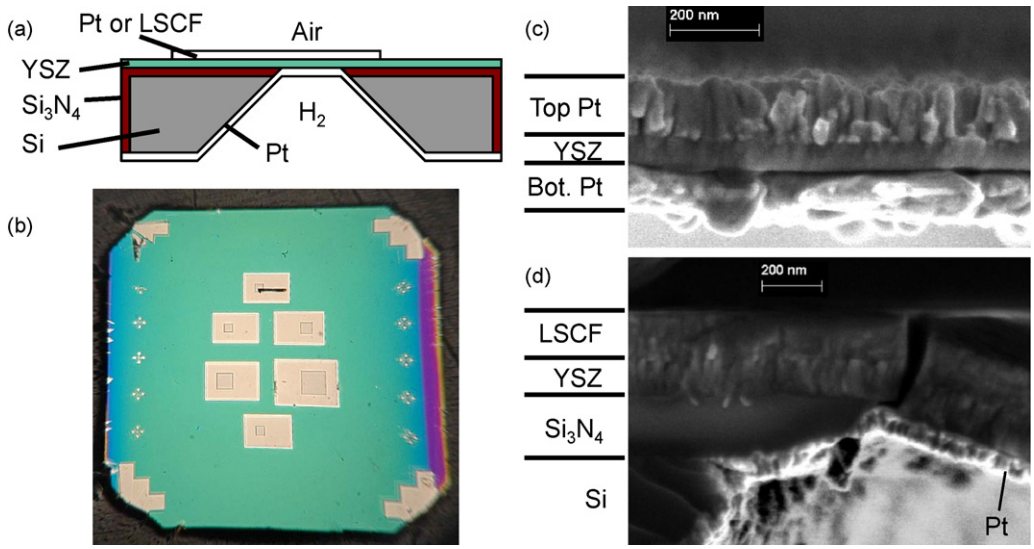

Fig. 2. Fuel cell structure. (a) Schematic of a cell. (b) Optical image of one 10-mm chip, containing six cells ranging in size from 80 to 500 μm. (c) Cross-sectional electron micrograph of a Pt–YSZ–Pt (PYP) membrane. (d) Cross section of an LSCF–YSZ–Pt (LYP) membrane, showing the edge of the Si/Si_3N_4 support.

PG (Microchem Corp.). Because photoresist is present during sputtering, this technique restricts the substrate to room temperature during deposition, although in some cases we annealed the YSZ in air at 800 °C for 2 h after liftoff but before Pt deposition. In other cases the chip was simply heated to 600 °C for measurement, and resistance was measured while cooling from there. Thin layers of other materials (particularly silicon nitride) may be sputtered into the same pattern either before or after YSZ deposition in order to change the bottom or top interface respectively and look for altered ionic conductivity. Dense Pt contact pads with Ti sticking layers were sputtered and patterned by photolithography and liftoff. Finally, porous Pt electrodes were sputtered, also patterned by photolithography and liftoff, connecting each side of an YSZ rectangle to a Ti/Pt contact pad, leaving a square of YSZ exposed. Each chip contains YSZ squares ranging from 20 to 500 μm on a side. A Si_3N_4 layer over the YSZ might be expected to interfere with the porous Pt electrodes, however we make this layer thin enough (5–10 nm) that it has sufficient defects to allow Pt/YSZ contact.

Fig. 1(b) shows the second in-plane device geometry. A blanket layer of YSZ is sputtered over a SiO_2-coated silicon chip. This is followed by patterning porous Pt strip electrodes via photolithography, sputtering, and liftoff. These strips are either 2 or 8 mm long, 500 μm wide, and separated by gaps of 10–200 μm. As the gap aspect ratios range from 10 to 800, fringing and interaction with other electrodes is ignored even though the YSZ covers the entire surface, unlike the devices in Fig. 1(a). The primary advantage of this geometry is that resistance is reduced by the gap aspect ratio, allowing measurement of far smaller conductivities and thus substantially lower temperatures. During device fabrication we found that Pt sticks substantially better to YSZ than to SiO_2 or Si_3N_4, such that simple porous Pt pads work well for these devices and for fuel cells, whereas in Fig. 1(a) the porous Pt may peel off the SiO_2 but is held on one side by YSZ and on the other by Ti/Pt.

2.3. Silicon nitride insulation devices

A slight modification to the design of Fig. 1(a) is to replace the thermal SiO_2 insulating the silicon chip with low-pressure chemical vapor deposition (LPCVD) silicon nitride. This was in fact the first type of device we fabricated for in-plane conductivity measurements, because Si_3N_4 is preferable to SiO_2 in fuel cell devices for two reasons. First, LPCVD Si_3N_4 is superior to SiO_2 as an etch mask, having selectivity in excess of 10,000:1 in standard KOH etches compared to only about 100:1 for SiO_2. Second, Si_3N_4 is a good diffusion barrier for silicon [17–19]. YSZ can be poisoned by small amounts of silicon incorporation [20], and although the Si_3N_4 is removed from the membrane prior to operation, any high-temperature processing before this step could allow silicon diffusion if no barrier were present. However, due to additional features in high-temperature impedance spectra resulting from this silicon nitride layer, it could not be used as the primary insulator for in-plane devices. Using Pt pads with no contact to YSZ we isolate and discuss these impedance spectra features.

2.4. Fuel cells

Thin-film fuel cells, shown in Fig. 2, were fabricated on silicon wafers using a sequence similar to that described by Huang et al. [5]. Each chip contained 6 square cells, ranging in size from 80 to 600 μm. We begin with silicon wafers coated by 200 nm low-stress LPCVD silicon nitride on both sides. 75–150 nm of YSZ was sputtered from a $Y_{0.08}Zr_{0.92}O_{1.96}$ target in 5 mTorr Ar and deposited at 1.0 nm min^{-1}, with the substrate at 550 °C. For LSCF cathodes, this was followed by sputtering 15–150 nm of LSCF from a $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ target, in 5 mTorr Ar at 1.0 nm min^{-1}. At this point some chips were taken out to analyze the LSCF (see Section 2.5). To pattern LSCF after deposition, S1813 is spun onto the chip and baked. The pattern is exposed through a photomask and developed in CD-26, and the exposed LSCF is etched away in a 2:5 mixture of hydrochloric acid and water. For porous Pt cathodes, YSZ deposition was followed by photolithography, Pt sputtering at room temperature in 75-mTorr argon at 7 nm min^{-1}, and liftoff.

Square holes were patterned in the back side nitride using photolithography and reactive ion etch (RIE) with O_2 and CF_4. The chips were placed in KOH (30 wt.% in water, 80–100 °C) to etch pyramidal wells through the silicon, stopping at the front side nitride. During this etch each chip was sealed into a stainless steel and Teflon housing to protect the top and sides. The nitride under the YSZ membrane is then removed by RIE in pure CF_4, so that silicon etches faster than nitride, to avoid undercutting at the edge of the membrane. Finally, a porous Pt anode is sputtered on the entire back surface.

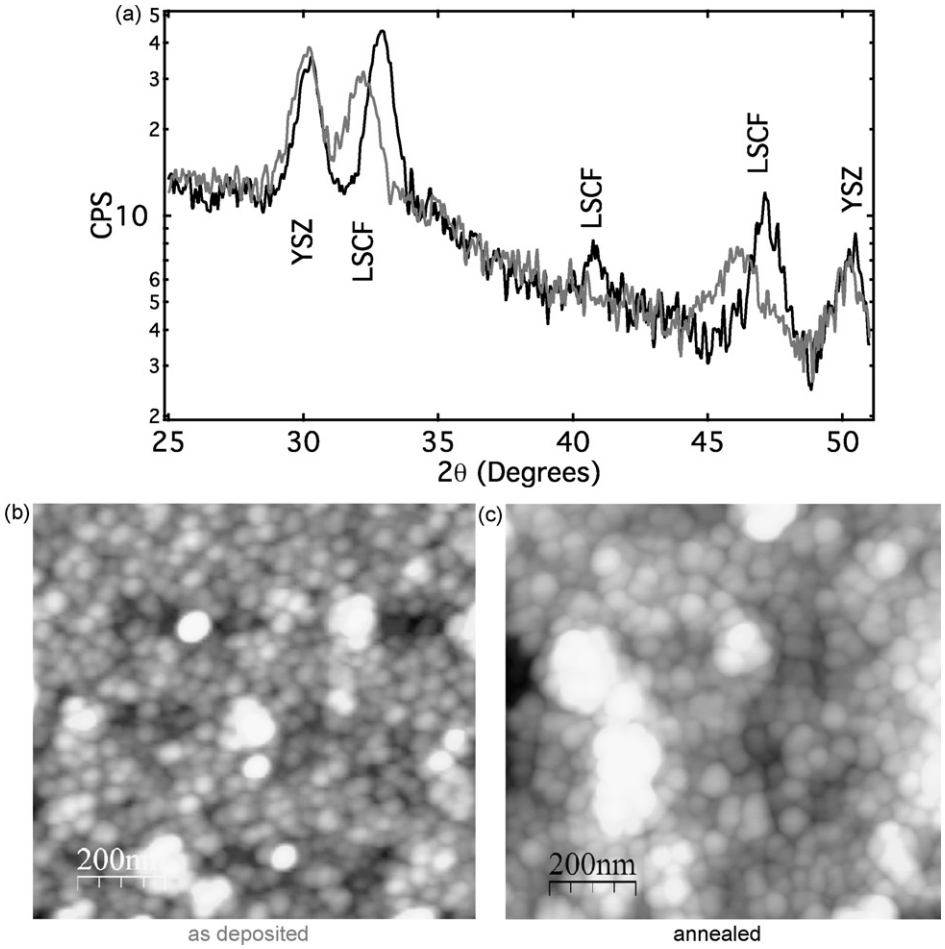

Fig. 3. X-ray diffraction spectra and atomic force micrographs before (gray) and after (black) annealing Si wafer with 200 nm Si_3N_4, 50 nm YSZ, and 60 nm LSCF.

2.5. LSCF electrode morphology

The structure of an LSCF film sputtered onto a YSZ film was characterized by X-ray diffraction (XRD) and atomic force microscopy (AFM) before and after annealing for 2 h at 600 °C in air. Fig. 3 shows the results for a device with 50 nm YSZ and 60 nm LSCF. The YSZ peaks in the XRD spectra are as expected and do not change on annealing. The LSCF is crystalline as deposited, but its peaks shift and narrow during annealing. The amount of shift implies a 2.1% contraction of the lattice, likely due to incorporation of additional oxygen or to release of film stress upon annealing. No extra peaks, for example due to reaction between LSCF and YSZ, are seen in the spectra [21], within the resolution of our measurement. On timescales up to several hours as we use here, other reports [16,22] also indicate that no interface reaction occurs below approximately 800 °C. AFM images show dense films with surface roughness increasing slightly from 3.6 to 4.7 nm RMS upon annealing and crystallite size also increasing slightly, consistent with the XRD peaks narrowing. Further structural and temperature-dependent electrical measurements of LSCF cathodes are reported in detail elsewhere [21].

2.6. Pt electrode morphology

Fig. 4 shows scanning electron microscope (SEM) images of Porous Pt films after various amounts of annealing. We begin with a 100-nm thick Pt film sputtered in 75 mTorr of argon, which produces the roughly 20 nm grains seen in Fig. 4(a). In general, these films exhibit grain size approximately one fifth the film thickness over a range of thicknesses and deposition rates, for argon pressures of 25 mTorr and greater. Upon annealing at elevated temperatures, the grains first coarsen (Fig. 4(b)), then large pores open as the grains coarsen further (Fig. 4(c) and (d)). These pores then begin to merge into larger openings (Fig. 4(e)) which eventually merge, breaking the Pt film into isolated lumps such that the film becomes insulating (Fig. 4(f)). This transition happens after a few hours at 600 °C, although the kinetics depends on a number of material parameters. Thinner films anneal faster, films on SiO_2 and Si_3N_4 anneal faster than those on YSZ, and contamination of the surface on which the Pt is deposited can cause accelerated annealing. The transition time is also affected by porosity: a dense film (deposited in low-pressure argon) will take substantially longer or higher temperature to break up, and a less porous film, such as one deposited inside a small etch hole (for example, the bottom Pt layer shown in Fig. 2(c)) will exhibit intermediate behavior. Another effect occurs inside etch holes as well: at the edge of a membrane, where flat YSZ transitions to sloped silicon via the Si_3N_4 layer, there may be a gap in the Pt layer. This is shown as deposited in Fig. 4(g), and persists after annealing as shown in Fig. 4(h). Notice that the as-deposited film on the membrane already looks like the partially annealed film in Fig. 4(b). This may reflect heating during deposition, since this deposition occurs on a thin membrane with little thermal mass to absorb energy from the Pt.

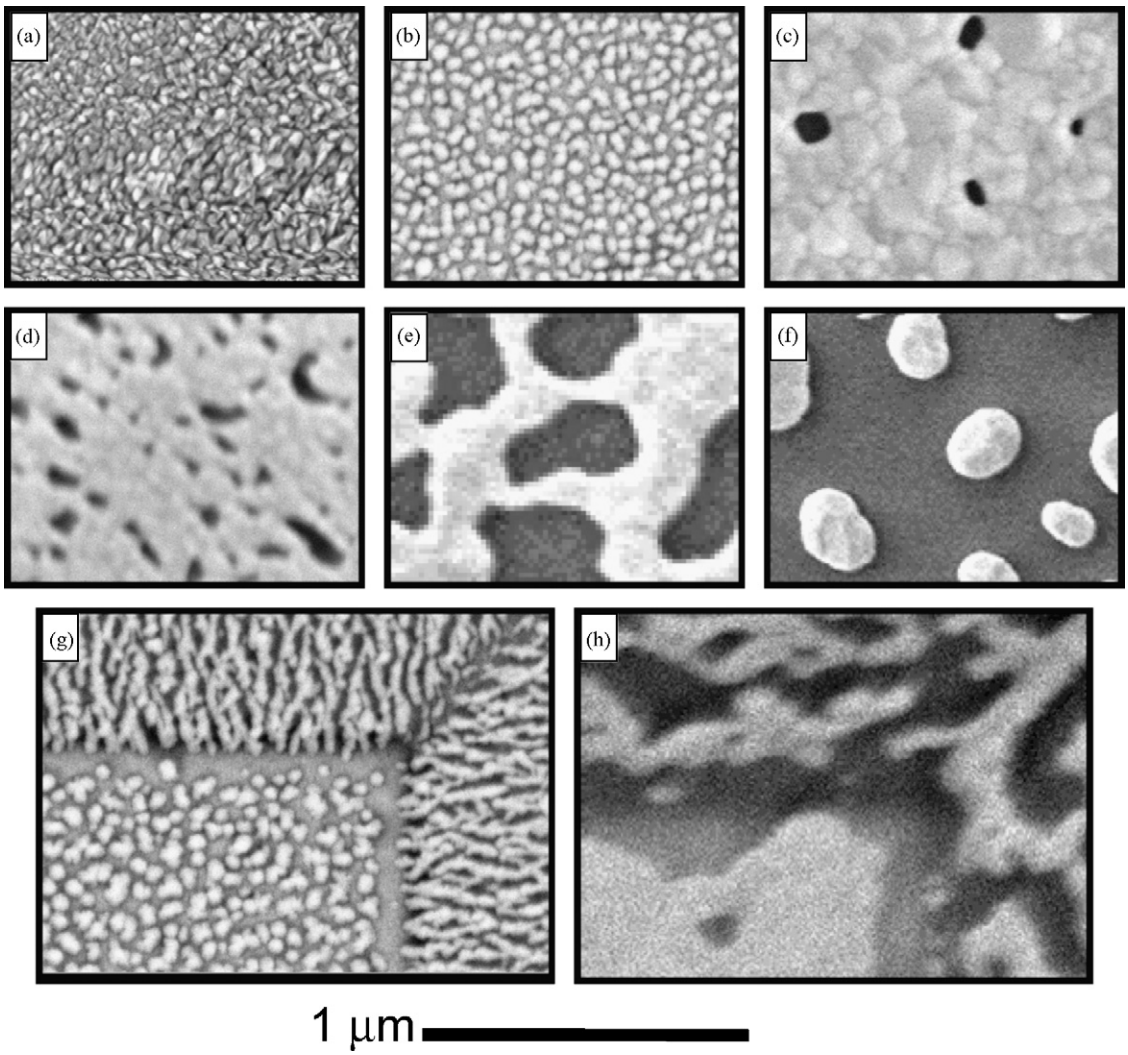

Fig. 4. The stages of annealing a sputtered porous Pt film. (a) As deposited, (b) grain coarsening, (c–e) formation and growth of large pores, and (f) loss of connectivity. At the edge of an etch hole the film can be discontinuous (g) as deposited with increased gap (h) after annealing.

3. Results and discussion

3.1. Electrolyte conductivity

The wide variety of measurements and observations in the literature concerning ionic conductivity in nanoscale films make it clear that the microstructure and synthesis of these films plays a crucial role in their performance [7,9,23,24]. With this in mind we measured the conductivity of YSZ films prepared in various conditions likely to be encountered in silicon-chip-based SOFCs, including thicknesses of 20–180 nm, bottom interfaces of SiO_2 and Si_3N_4, and top interfaces of Si_3N_4 and air. Impedance spectroscopy measurements were performed on each device as a function of temperature. Due to the conductive silicon wafer under the SiO_2 insulation in each device, only a single semicircle was seen in each spectrum, with frequency response dominated by the capacitance from one contact pad to the other through the silicon wafer. Thus an overall conductivity value could be extracted from each measurement, and it was not possible to determine whether separate bulk and grain boundary contributions were present. Similar impedance spectra have been observed by other researchers investigating in-plane conductivity of thin-film oxide-ion conductors [7,11]. The results are displayed in Fig. 5, from 450 to 600 °C in Fig. 5(a) and the full data set in Fig. 5(b). The highest and lowest conductivities measured at any given temperature differ by roughly a factor of 4 (see Fig. 5(a)). Activation energies range from 0.77 eV for 180 nm OYN (oxide below, 180 nm YSZ, and nitride above) to 1.09 eV for 180 nm OYA (oxide–YSZ–air), with a single activation energy describing each film over its entire temperature range (see Fig. 5(b)). Despite these variations, no clear trends were observed as functions of top or bottom interface or annealing, within the ranges explored. These conductivities are somewhat smaller than previously reported values for thin film and bulk single crystal YSZ [6–11], although polycrystalline YSZ has been observed to have even lower conductivity [25]. Further work is necessary to determine the causes of the lower conductivity we observe, but we note that the conductivity values measured here are sufficient for enhanced fuel cell performance given a submicron membrane.

3.2. Silicon nitride insulation layer

Fig. 6(a) shows the probe geometry for measuring impedance spectra of Si_3N_4 insulation layers at high temperatures. Probes are connected to two 15.2 mm^2 Pt pads that make no contact to YSZ, and therefore are expected to function simply as two capacitors connected in series via the silicon chip (equivalent to one 7.6 mm^2

capacitor). Fig. 6(b) and (c) shows the magnitude and phase of the impedance spectrum of this structure for five temperatures from 210 to 576 °C. At room temperature the device looks like a pure capacitor, as expected, but as the temperature increases a series of three plateaus appear in the magnitude, dropping rapidly as temperature increases. Along with each plateau in magnitude comes a dip in phase, characteristic of a lumped resistor–capacitor element in an equivalent circuit. Arrows highlight these plateaus/dips for the 576 °C data. The solid curves are fits of each data set to a phenomenological model with three RC elements (Fig. 7(a)). Fig. 7(b) and (c) gives the values of each resistor and capacitor extracted from these fits vs. inverse temperature, with the corresponding Celsius scale shown on top. The first two resistors are well described by thermal activation functions (solid lines), with activation energies of 1.12 and 0.74 eV, respectively. The third, which has a much higher resistance and is only visible at the highest two temperatures measured, is consistent with an activation energy around 0.8 eV. The capacitances show only slight variation with temperature, rising as temperature increases.

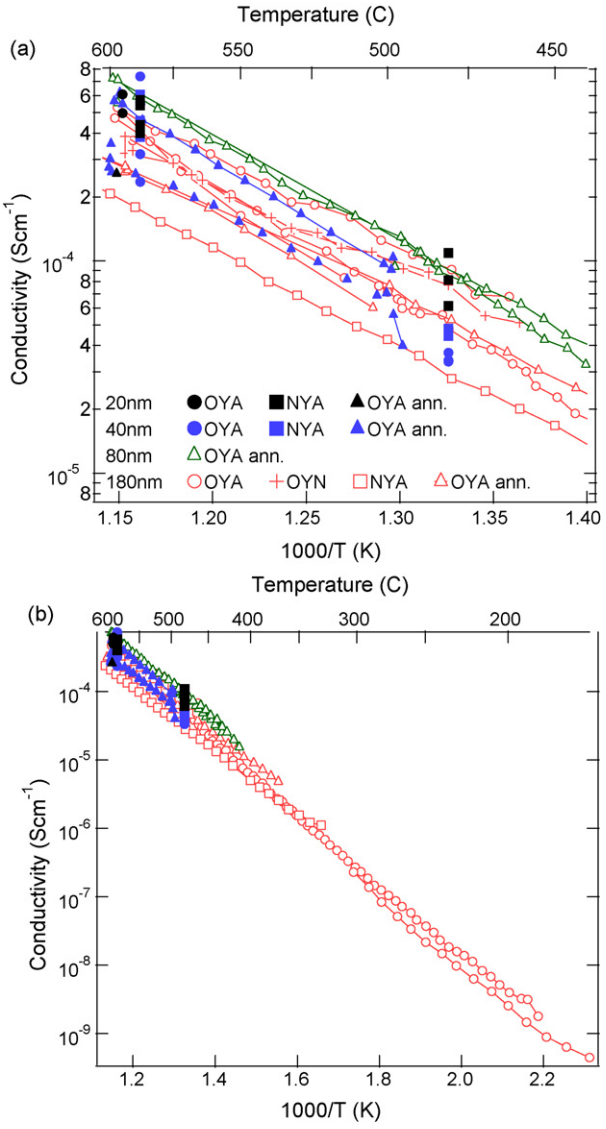

Fig. 5. In-plane conductivity of YSZ with various thicknesses and interfaces vs. inverse temperature, with the corresponding Celsius scale on top. (a) Zoom in of the high-temperature region and (b) full data set. O = SiO_2, N = Si_3N_4, Y = YSZ and A = air.

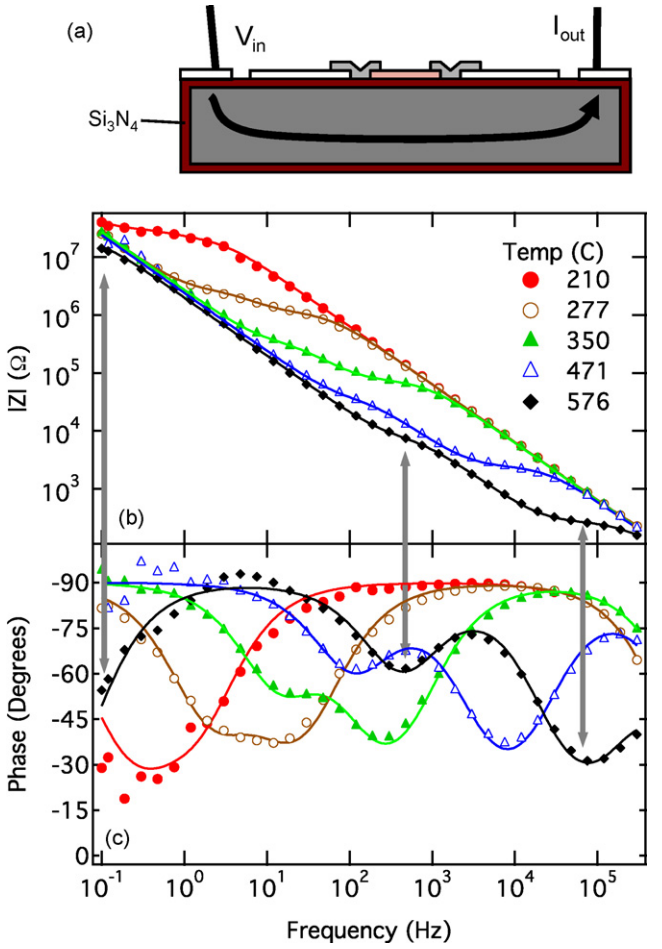

Fig. 6. Impedance spectroscopy of Pt/Si_3N_4/Si capacitor structure at various temperatures. (a) Device schematic, (b) magnitude and (c) phase of impedance vs. frequency. Points are data, curves are fits to an empirical model. Model parameters are plotted in Fig. 7. Gray arrows from (b) to (c) highlight magnitude plateaus and phase dips at 576 °C.

Although the physical origin of these three plateaus is unknown, several observations indicate that these complex impedance spectra are intrinsic to LPCVD silicon nitride. The same spectra have been observed in a number of devices made with both commercial and in-house grown nitride films but never seen in devices insulated by thermally grown SiO_2. These features are independent of pinhole density. Pinholes in the nitride cause drastic pitting in wet etching tests but electrically they either short the device entirely or have no effect on the impedance spectra. Finally, at least the first two RC elements and the third capacitance are unchanged if the Pt electrodes are replaced by gold (gold films do not withstand high enough temperatures to observe the third resistance). The effect on fuel cell measurements therefore is significant: silicon nitride is a better choice for an insulating barrier below the YSZ for silicon-chip-based SOFCs, but if it is used, impedance spectroscopy on a cell becomes challenging to use to investigate electrode and electrolyte properties, and only DC measurements produce reliable results. These observations are critical for understanding functional properties of thin-film SOFC devices fabricated on silicon substrates.

3.3. Fuel cell measurements

Table 1 describes the five fuel cells used in this study, including three LSCF/YSZ/Pt cells (LYP1-3) and two Pt/YSZ/Pt cells (PYP1 and 2). Fig. 8 presents the (a) maximum specific power and (b)

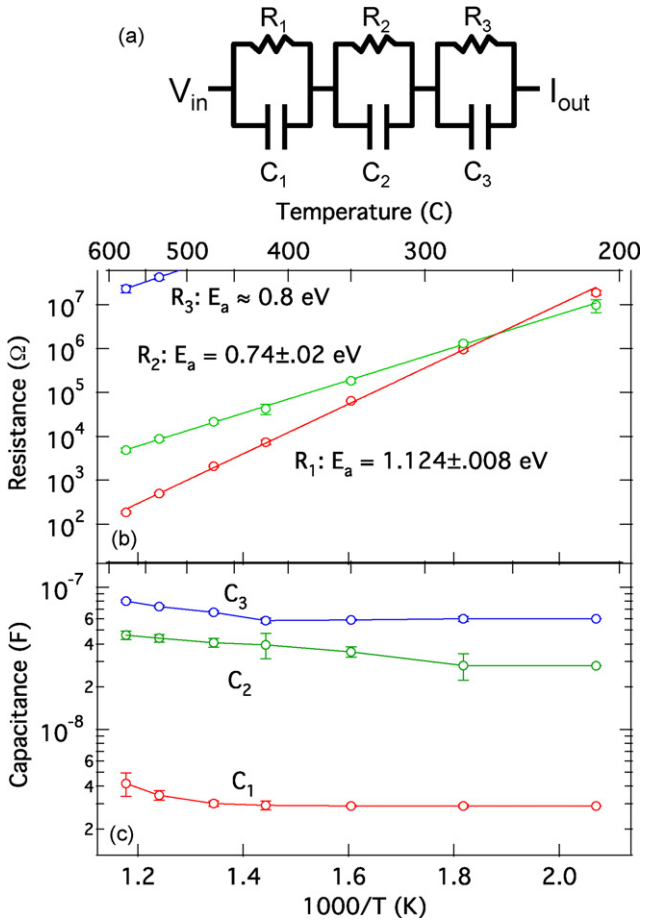

Fig. 7. Model and fit parameters for impedance spectroscopy of Pt/Si_3N_4/Si data. (a) Equivalent circuit schematic, (b) resistance and (c) capacitance elements vs. inverse temperature. Curves in (b) are Arrhenius activation fits to each resistance element.

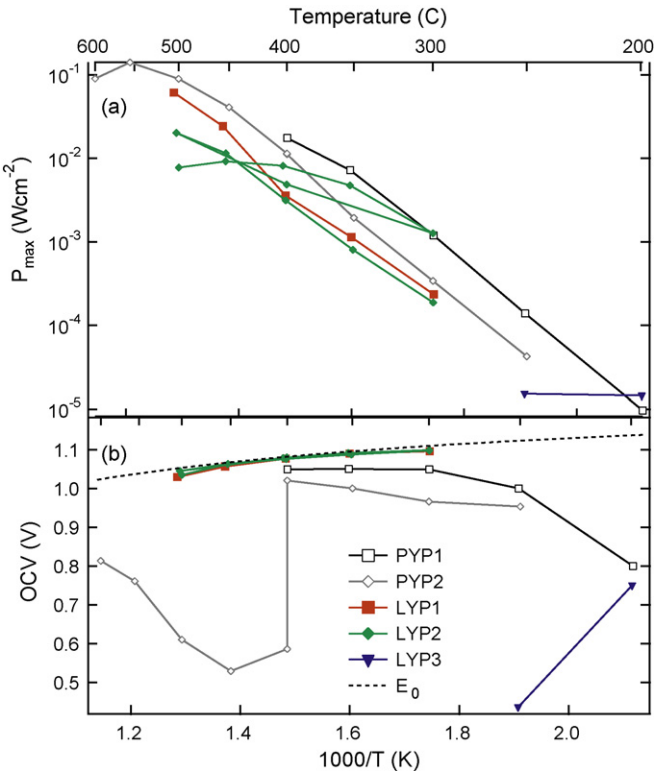

Fig. 8. Performance of Pt/YSZ/Pt (PYP) and LSCF/YSZ/Pt (LYP) fuel cells. (a) Maximum specific power and (b) open circuit voltage (including the Nernst potential E_0) vs. inverse temperature, with the corresponding Celsius scale on top.

open circuit voltage (OCV) of each cell vs. temperature. Fig. 9 shows some of the current/voltage curves from which these values were extracted, and Fig. 10 displays the same data against a logarithmic current axis to highlight the low-current behavior dominated by electrode kinetics. At most temperatures the Pt-cathode cells produced the greatest power, with several notable exceptions which are encouraging for further development. In particular, our measurements of LYP1 and LYP2 indicate that LSCF can tolerate high temperatures better than Pt, and LYP2 and LYP3 raise the possibility of LSCF outperforming Pt cathodes for thin-film SOFCs.

PYP2 produced the highest power we measured, 141 mW cm^{-2} at 550 °C, before degrading as we increased temperature to 600 °C. At 500 °C, LYP1 (60 mW cm^{-2}) produced only slightly less power than PYP2 (90 mW cm^{-2}). PYP1 was measured only up to 400 °C, and showed the best performance over much of this range, although at 200 and 300 °C, the best were LYP3 (15 μW cm^{-2}) and LYP2 (1.3 mW cm^{-2}) respectively. Except LYP2, all measurements shown were taken while increasing temperature. Device LYP1 degraded only slightly after 3 h at 400–500 °C, and LYP2 improved substantially during the first thermal cycle (also 3 h at 400–500 °C) before degrading in the second.

Table 1
Fuel cell device parameters.

Cell	Cathode (nm)	YSZ (nm)	Pt anode (nm)	Width (μm)
PYP1	130 Pt	75	80	80
PYP2	130 Pt	75	80	80
LYP1	15 LSCF	75	40	80
LYP2	15 LSCF	75	40	350
LYP3	150 LSCF	150	80	80

Although numerous processes affect maximum power, the temperature dependence of maximum power output from each cell fits fairly well to a single activation energy over about two orders of magnitude (leaving aside LYP3 due to its severe degradation before sufficient data could be acquired). PYP1 and 2 give 1.06 and 1.09 eV and LYP1 and 2 give 1.03 and 0.94 eV, respectively. Although these are in the expected range for YSZ, the power is below the electrolyte limit. Most of the *I–V* curves for both types of cell are linear in Fig. 10 (meaning that current is exponential in overpotential) from just below OCV down to 0.4 V or lower. This implies that electrode kinetics are a dominant loss mechanism, although prior reports place the activation energy of catalysis by LSCF substantially higher (1.3–1.6 eV) [16,26].

Current collection losses may account for the divergence in maximum power output between LYP1 and LYP2 (first heating) above 400 °C. At 500 °C, our thicker LSCF films had electronic conductivities around 700 S cm^{-1}, but in films under 30 nm conductivity was nearly an order of magnitude lower [21]. To model cathode current collection we estimate that, on average, current travels through a cross section $2wt$ for a distance $w/4$, with w the cell width and t the cathode thickness. Restricting ohmic loss to 0.1 V, any single region of 15-nm LSCF at 70 S cm^{-1} may only collect 20 μW, or 20 mW cm^{-2} for LYP2 but 0.3 W cm^{-2} for the smaller LYP1. From nearly equal power (3 mW cm^{-2}) at 400 °C, LYP1 rises to 61 mW cm^{-2} at 500 °C while LYP2 rises only to 20 mW cm^{-2}, in line with the current collection limit. The *I–V* curves for LYP1 and LYP2(i) at 500 °C (Fig. 9(d)) look similar at low current (very similar OCV and initial curvature) but diverge roughly linearly at higher currents, consistent with this ohmic loss from current collection. This may also explain the dif-

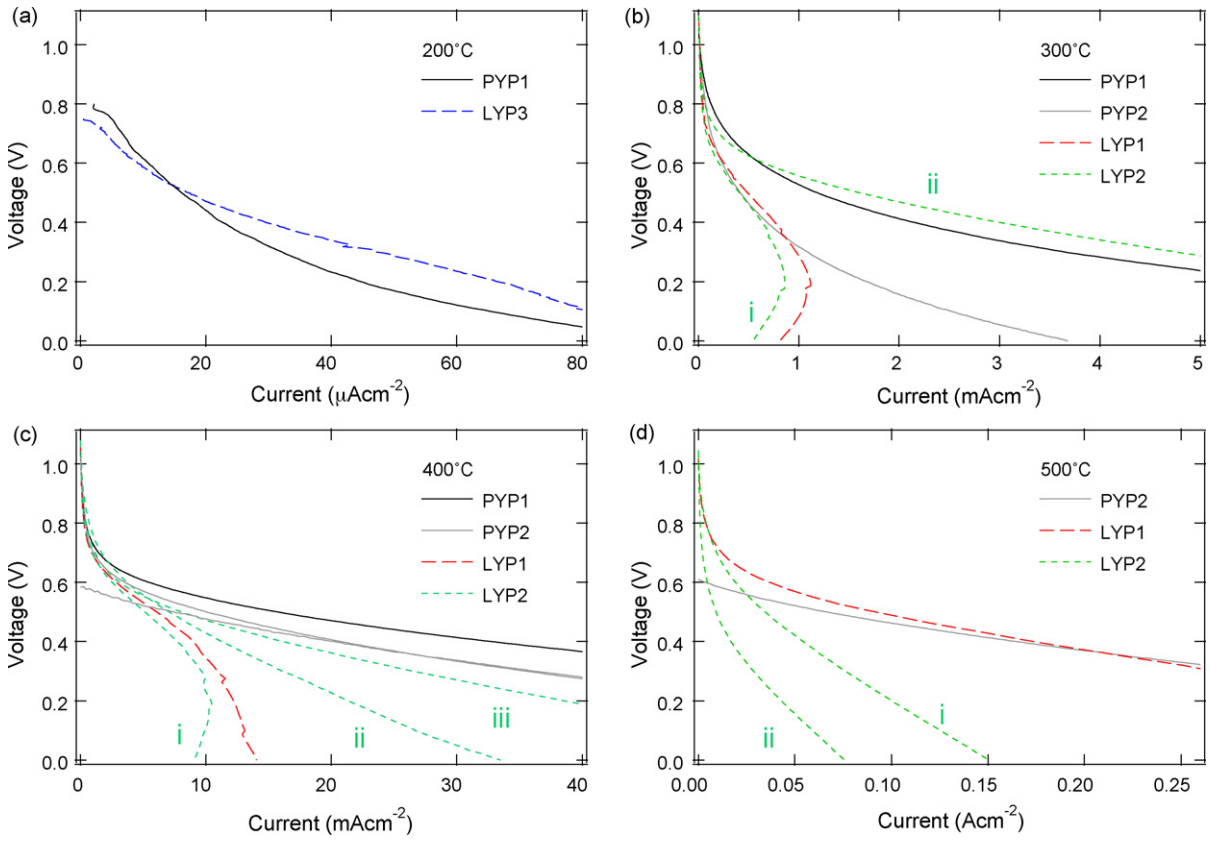

Fig. 9. Current/voltage sweeps for various cells at (a) 200 °C, (b) 300 °C, (c) 400 °C, and (d) 500 °C. For LYP2, Roman numerals denote sweeps during (i) the first heating, (ii) cooling, and (iii) second heating. At 400 °C (c), two traces of PYP2 are shown, before and after an OCV drop.

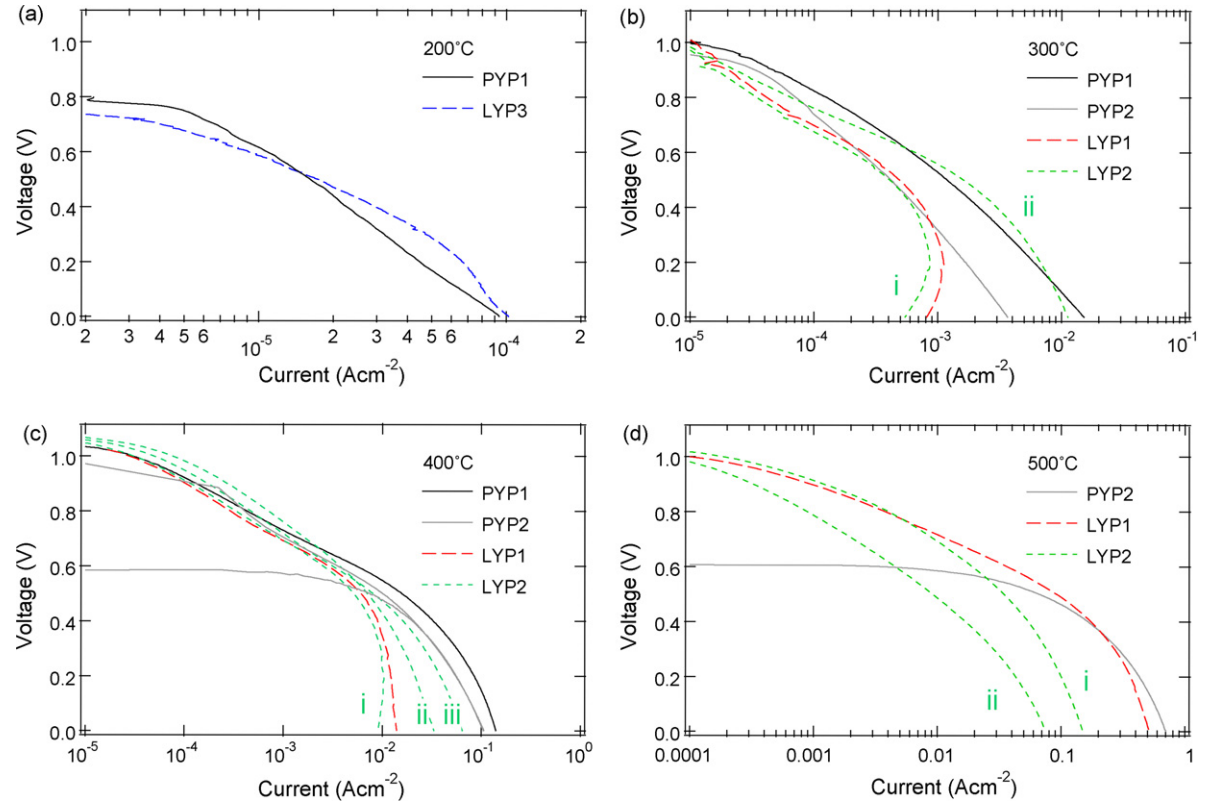

Fig. 10. The same data as Fig. 9 against a logarithmic current axis.

ference in maximum power activation energy between LYP1 and 2.

Between 350 and 450 °C, LYP1 and 2 have OCVs within 10 mV of the thermodynamic limit (dashed curve in Fig. 8b), and within 25 mV at 300 and 500 °C. PYP1 and 2, however, are at least 30 mV and often over 100 mV below the limit. Moreover, some Pt-cathode cells abruptly and irreversibly drop to much lower OCV, as PYP2 did at 400 °C—the two PYP2 curves in Fig. 9(c), for example, were taken minutes apart. Both before and after such a drop, OCV increases with temperature, indicating electronic or gaseous leakage that is less temperature dependent than ionic resistance. These drops are not correlated with mechanical breakdown, implying that Pt diffusion, possibly via grain boundaries or pinholes in the YSZ, may form partial electrical shorts. In contrast, OCV drops in LSCF-cathode cells tend to presage visible cracks, implying that small cracks and gas leakage cause these drops. LYP3 outperformed PYP1 at 200 °C despite an already lower OCV, implying that if these mechanical constraints can be addressed LSCF can be expected to outperform Pt as a cathode material throughout the intermediate temperature range.

A close examination of Fig. 9(c) provides some insight into the performance differences between cells with LSCF and Pt cathodes. An unusual effect is observed which, if it can be understood, may lead to substantially improved power output. Each current-voltage sweep was taken by fixing voltage and measuring current. At low current they all look similar (except for the second measurement of PYP2, after its OCV dropped). LYP1 and LYP2 have slightly higher OCV and exchange current (20–50 $\mu A\,cm^{-2}$ vs. 10 $\mu A\,cm^{-2}$ for PYP1) but lower transfer coefficient (0.53–0.63 vs. 0.72 for PYP1). However, at higher current a reversible time- and voltage-dependent loss affects LYP1 and LYP2. At voltages well below OCV, the current drops with time, in some cases curving the *I–V* sweep backward. Jumps in the data, visible for example on the LYP1 curve at around 0.25 and 0.1 V, are not noise but rather places current dropped more when the sweep paused during an update of the temperature controller. In one instance, the cell was left at $V = 0$ for 30 min and current decreased an order of magnitude. After this OCV was only 0.8 V, but recovered its initial value after 30 min at $I = 0$. After cycling to other temperatures, subsequent measurements of LYP2 at the same temperature this effect diminished, increasing power output substantially.

4. Conclusions

This study has demonstrated functional thin-film SOFCs with LSCF cathodes made by sputtering, etching, and lithography. To the best of our knowledge, this is the first report describing functional fuel cells with RF-sputtered LSCF ultra-thin films from a composite target. Maximum power output of $\sim$60 mW cm^{-2} was obtained at 500 °C with LSCF cathodes, which is comparable to results reported in the literature using similar micro-fabrication approaches utilizing ultra-thin-film oxides. Deposition techniques enabling rougher or porous LSCF surfaces could further improve performance by increasing the area for catalysis. Impedance characteristics of fully processed devices as well as various component layers have been analyzed as a function of temperature and presented. The results are encouraging towards the use of non-precious metal cathodes for low and intermediate temperature thin-film solid oxide fuel cells.

Acknowledgments

We thank Antonio Baclig, Amrita Saigal, and the Rowland Institute at Harvard staff for technical support. The authors acknowledge financial support from SiEnergy Systems, the Harvard University Center for the Environment, and the Eppley Foundation for Research.

References

[1] B.C.H. Steele, A. Heinzel, Nature 414 (2001) 345–352.
[2] S.M. Haile, Acta Mater. 51 (2003) 5981–6000.
[3] V.V. Kharton, F.M.B. Marques, A. Atkinson, Solid State Ionics 174 (2004) 135–149.
[4] C.D. Baertsch, K.F. Jensen, J.L. Hertz, H.L. Tuller, S.T. Vengallatore, S.M. Spearing, M.A. Schmidt, J. Mater. Res. 19 (2004) 2604–2615.
[5] H. Huang, M. Nakamura, P. Su, R. Fasching, Y. Saito, F.B. Prinz, J. Electrochem. Soc. 154 (2007) B20–24.
[6] A. Bieberle-Hutter, D. Beckel, A. Infortuna, U.P. Muecke, J.L.M. Rupp, L.J. Gauckler, S. Rey-Mermet, P. Muralt, N.R. Bieri, N. Hotz, M.J. Stutz, D. Poulikakos, P. Heeb, P. Muller, A. Bernand, R. Gmur, T. Hocker, J. Power Sources 177 (2008) 123–130.
[7] I. Kosacki, C.M. Rouleau, P.F. Becher, J. Bentley, D.H. Lowndes, Electrochem. Solid-State Lett. 7 (2004) A459–A461.
[8] S. Azad, O.A. Marina, C.M. Wang, L. Saraf, V. Shutthanandan, D.E. McCready, A. El-Azab, J.E. Jaffe, M.H. Engelhard, C.H.F. Peden, S. Thevuthasan, Appl. Phys. Lett. 86 (2005) 131906.
[9] X. Guo, E. Vasco, S. Mi, K. Szot, E. Wachsman, R. Waser, Acta Mater. 53 (2005) 5161–5166.
[10] H. Huang, T.M. Gur, Y. Saito, F.B. Prinz, Appl. Phys. Lett. 89 (2006) 143107.
[11] A. Karthikeyan, C.-L. Chang, S. Ramanathan, Appl. Phys. Lett. 89 (2006) 183116.
[12] J. Garcia-Barriocanal, A. Rivera-Calzada, M. Varela, Z. Sefrioui, E. Iborra, C. Leon, S.J. Pennycook, J. Santamaria, Science 321 (2008) 676–680.
[13] J.H. Shim, C.-C. Chao, H. Huang, F.B. Prinz, Chem. Mater. 19 (2007) 3850–3854.
[14] L.-W. Tai, M.M. Nasrallah, H.U. Anderson, D.M. Sparlin, S.R. Sehlin, Solid State Ionics 76 (1995) 259–271.
[15] Z. Shao, S.M. Haile, Nature 431 (2004) 170–173.
[16] F.S. Baumann, J. Fleig, G. Cristiani, B. Stuhlhofer, H.-U. Habermeier, J. Maier, J. Electrochem. Soc. 154 (2007) B931–B941.
[17] A.E. Kaloyeros, E. Eisenbraun, Annu. Rev. Mater. Sci. 30 (2000) 363–385.
[18] G. Bilger, T. Voss, T. Schlenker, A. Strohm, Surf. Interface Anal. 38 (2006) 1687–1691.
[19] H. Schmidt, U. Geckle, M. Bruns, Phys. Rev. B 74 (2006) 045203.
[20] J.L. Hertz, A. Rothschild, H.L. Tuller, J. Electroceram. (2008), doi:10.1007/s10832-008-9475-5.
[21] B.-K. Lai, A.C. Johnson, H. Xiong, S. Ramanathan, J. Power Sources 186 (2009) 115–122.
[22] S.P. Simner, M.D. Anderson, M.H. Engelhard, J.W. Stevenson, Electrochem. Solid-State Lett. 9 (2006) A478–A481.
[23] J.H. Joo, G.M. Choi, Solid State Ionics 177 (2006) 1053–1057.
[24] X. Guo, R. Waser, Prog. Mater. Sci. 51 (2006) 151–210.
[25] N.Q. Minh, T. Takahashi, Science and Technology of Ceramic Fuel Cells, Elsevier, Amsterdam, 1995, p. 94.
[26] S.P. Jiang, Solid State Ionics 146 (2002) 1–22.